HIGH DATA RATE DIFFERENTIAL SIGNAL LINE DESIGN FOR UNIFORM CHARACTERISTIC IMPEDANCE FOR HIGH PERFORMANCE INTEGRATED CIRCUIT PACKAGES

ABSTRACT OF THE DISCLOSURE

Provided is an apparatus that includes an integrated circuit (IC) mounted on a chip carrier. The IC has one or more differential pair circuits coupled thereto and the chip carrier has a signal escaping portion and a remaining portion. The apparatus also includes differential signal lines coupled to the differential pair circuits, the differential signal lines (i) extending through the chip carrier and (ii) having first and second segments. The first segment extends through the escaping portion and the second segment extends through the remaining portion. The first and second segments have respective first and second widths.